UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

H·A

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,371	02/26/2004	YI-JEN CHAN	11955-US-PA	2370

31561 7590 02/01/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, LINH V	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,371	CHAN ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to RCE filed on 1/11/07. Claims 1, 7 and 13 have been amended. Claims 16 – 17 have been added. Claims 1 – 17 are pending on this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1- 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa et al. U.S. patent No. 5,982,236.

Regarding claim 1, Fig. 17 of Ishikawa et al. discloses a power amplifier (Trb) with an active bias circuit (D1, C1, R1- R4, Cb, Vc), comprising: a power amplifier transistor (Trb) with a gate (gate of Trb) connected to a gate bias voltage (D); and an active bias circuit (D1, C1, R1- R4, Cb, Vc), connected to an input power terminal (E) and the gate of the power amplifier transistor (Gate of Trb) for receiving an input power (output of 3) from the input power terminal (E) and outputting the gate bias voltage (D), to the gate wherein the gate bias voltage (gate of Trb) is increased corresponding to an increase of the input power (Col. 12 lines 25 – 30), wherein the active bias circuit comprises a voltage source (Vc).

Regarding claim 4, wherein the power amplifier transistor (Trb) and the active bias circuit (D1, C1, R1- R4, Cb, Vc), is manufactured by a system on chip process (Fig. 17).

Regarding claim 5, wherein the active bias circuit (4) comprises a diode (D1) and a resistor (R1 – R4).

Regarding claim 6, wherein an equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor D1, because the output of D1 varies according to RF input power (E) therefore the equivalent resistance of D1 must be varies according to power input E).

Regarding claim 7, Fig. 1 of Ishikawa et al Fig. 17 of Ishikawa et al discloses an integrated circuit for a power amplifier (Trb) with an active bias circuit (D1, C1, R1- R4, Cb, Vc), comprising: a power output device (output terminal of 3); a power amplifier transistor (Trb) with a gate (Gate of Trb) connected to a gate bias voltage (voltage bias D; an active bias circuit (D1, C1, R1- R4, Cb, Vc), connected to the power output device (output terminal 3) and the gate of the power amplifier transistor (gate of Trb) for receiving an input power (E) from the power output device (output terminal of 3) and providing a gate bias voltage (D) to the gate (gate of Trb), wherein the gate bias voltage (4) is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28),), wherein the active bias circuit comprises a voltage source (Vc); and a power input device (input terminal of 3) connected to an output terminal (output terminal of Trb)

of the power amplifier transistor (Trb) for receiving an amplified output power (amplified output power of Trb) from the power amplifier transistor (Trb).

Regarding claim 10, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip process (Fig. 17).

Regarding claim 11, wherein the active bias circuit (D1, C1, R1- R4, Cb, Vc), comprises a diode (D1) and a resistor (R1 – R4).

Regarding claim 12, wherein the equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor D1, because the output of D1 varies according to RF input power (E) therefore the equivalent resistance of D1 must be varies according to power input E).

Regarding claim 13, Fig. 17 Ishikawa et al. discloses method for generating a gate bias voltage (B) of a power amplifier transistor (Trb) corresponding to an input power (E), comprising: providing an input power (E); and outputting a gate bias voltage (D) corresponding to the input power (E), wherein the gate bias voltage (D1, C1, R1-R4, Cb, Vc), is powered by a voltage source (Vc) other than the input power (E) is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28).

Regarding claims 2 - 3, 8 - 9 and 14 – 15, wherein a curve of an increase of the gate bias voltage versus the input power is a linear or non-linear curve (Ishikawa et al. as applied to claims 1, 7 and 13 above disclosed the voltage bias for power amplifier transistor Trb is increase or decreasing according to increase or decrease of the Power input terminal E; therefore the curve of increase of the gate bias voltage of Ishikawa et

al. must be either in the form of linear or non-linear curve. Further more Fig. 18 of Ishikawa further discloses a linear and non-linear curve of Pout at the power input terminal E; hence, voltage bias increase or decrease according to increase or decrease of linear or non-linear of Pout; thereby, voltage bias (D) of power amplifier Trb must be increase or decrease linear or non-linear accordingly to increase or decrease of linear or non-linear of Pout at input power terminal E.

Regarding claims 16 and 17, wherein the active bias circuit (D1, C1, R1- R4, Cb, Vc) comprises a ground level (Ground).

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

1/26/07

Linh Van Nguyen

Art Unit 2819

LINH NGUYEN
PRIMARY EXAMINER